Remarks:

Reconsideration of the application is requested.

Claims 1-5 and 11-24 remain in the application. Claims 1 and 3 have been amended.

The changes to claims 1 and 3 are provided solely for formal and cosmetic reasons to avoid a possible contradiction with the subject-matter recited in claims 14 and 20. The changes are neither provided for overcoming the prior art nor do they narrow the scope of the claims for any reason related to the statutory requirements for a patent.

Respectfully submitted,

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For Applicants

MN:cgm

August 6, 2002

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Applic. No. : 09/761,594

Version with markings to show changes made:

Claim 1 (twice amended). A semiconductor device in chip format, comprising:

a chip;

electrical connection pads disposed on said chip;

at least one first insulating layer disposed on said chip such that said electrical connection pads are free of said first insulating layer on at least one surface;

interconnects running on said first insulating layer and in each case lead from said electrical connection pads to base regions;

a second insulating layer disposed on said interconnects and on said first insulating layer, said second insulating layer having a thickness, said second insulating layer having openings formed therein leading to said base regions;

a conductive material with an elasticity, introduced into each of said openings;

small balls [having a metallic coating on an outside and having an elasticity] disposed on said conductive material in a region of a free end of each of said openings, said small

balls having an elasticity and being metallic at least on an outside; and

said thickness of said second insulating layer, said elasticity of said conductive material, and said elasticity of said small balls resulting in a desired comparatively good mechanical decoupling from a printed circuit board upon the semiconductor component being soldered onto the printed circuit board.

Claim 3 (twice amended). A method for producing semiconductor devices in a chip format, which comprises:

providing chips;

placing electrical connection pads on the chips;

applying at least one first insulating layer to at least one surface of the chips such that the electrical connection pads are left at least partially uncovered by the first insulating layer;

producing interconnects on the at least one first insulating layer, the interconnects leading to base regions of external connection elements;

applying a second insulating layer on the interconnects and on the at least one first insulating layer, the second insulating layer having a thickness;

forming openings in the second insulating layer above the base regions and leading to the base regions;

introducing a conductive material with an elasticity into the openings;

placing small balls [having an elasticity and a metallic coating on the outside and having an elasticity] onto the conductive material in a region of a free end of each of the openings, said small balls having an elasticity and being metallic at least on an outside; and

the thickness of said second insulating layer, the elasticity of the conductive material, and the elasticity of the small balls resulting in a desired comparatively good mechanical decoupling from a printed circuit board upon the semiconductor component being soldered onto the printed circuit board.

Applic. No. : 09/761,594

Version with markings to show changes made:

Claim 1 (twice amended). A semiconductor device in chip format, comprising:

a chip;

electrical connection pads disposed on said chip;

at least one first insulating layer disposed on said chip such that said electrical connection pads are free of said first insulating layer on at least one surface;

interconnects running on said first insulating layer and in each case lead from said electrical connection pads to base regions;

a second insulating layer disposed on said interconnects and on said first insulating layer, said second insulating layer having a thickness, said second insulating layer having openings formed therein leading to said base regions;

a conductive material with an elasticity, introduced into each of said openings;

small balls [having a metallic coating on an outside and having an elasticity] disposed on said conductive material in a region of a free end of each of said openings, said small

balls having an elasticity and being metallic at least on an outside; and

said thickness of said second insulating layer, said elasticity of said conductive material, and said elasticity of said small balls resulting in a desired comparatively good mechanical decoupling from a printed circuit board upon the semiconductor component being soldered onto the printed circuit board.

Comparative to what?

Claim 3 (twice amended). A method for producing semiconductor devices in a chip format, which comprises:

providing chips;

placing electrical connection pads on the chips;

applying at least one first insulating layer to at least one surface of the chips such that the electrical connection pads are left at least partially uncovered by the first insulating layer;

producing interconnects on the at least one first insulating layer, the interconnects leading to base regions of external connection elements;

applying a second insulating layer on the interconnects and on the at least one first insulating layer, the second insulating layer having a thickness;

the thickness of said second insulating layer, the elasticity of the conductive material, and the elasticity of the small balls resulting in a desired comparatively good mechanical decoupling from a printed circuit board upon the semiconductor component being soldered onto the printed circuit board.

Claim 4 (amended). The method according to claim 3, which comprises using a doctor blade for introducing the conductive material into the openings.

Claim 5 (amended). The method according to claim 19, which comprises

forming the chips on a wafer; and

after the curing of the conductive adhesive, dividing the wafer to obtain the semiconductor devices.

Claim 11 (amended). The method according to claim 18, which comprises:

forming the chips on a wafer; and

after the remelting of the solder paste, dividing the wafer to obtain the semiconductor devices.